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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,867	03/26/2004	Masanori Ueda	025720-00027	7607

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EXAMINER	
TUGBANG, ANTHONY D	
ART UNIT	**PAPER NUMBER**
3729	

MAIL DATE	DELIVERY MODE
06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

ED

Office Action Summary	Application No.	Applicant(s)	
	10/809,867	UEDA ET AL.	
	Examiner	Art Unit	
	A. Dexter Tugbang	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *5-10 and 14-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/15/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 20, 2007 has been entered.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

3. Claims 5 through 10 and 14 through 17 continue to stand as being withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 13, 2006.

Claim Rejections - 35 USC § 103

4. Claims 1 through 3, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Onishi et al 6,426,583, Chou 3,430,109, and Kawaura et al 4,426,595.

Regarding Claim(s) 1, Onishi discloses a method of fabricating a surface acoustic wave device (Figures 10A through 10E) comprising: joining a supporting substrate (e.g. 102a in Fig. 9A) to a second surface (bottom surface of 101a) of a piezoelectric substrate 101a opposite to a

first surface (top surface of 101a) of the piezoelectric substrate; grinding and polishing the first surface (top surface of 101a) of the piezoelectric substrate (in Fig. 10B, col. 10, lines 13-26 and col. 7, lines 49-56); forming, on the first surface of the piezoelectric substrate, on on-chip pattern including comb-shaped electrodes (e.g. 104); and grinding a third surface (top surface of 102a) to form grooves 202 of the supporting substrate opposite to another surface (through to bottom surface of 102a in Fig. 10E) of the supporting substrate to which the second surface (bottom surface of 101a) of the piezoelectric substrate is joined, after forming the on-chip pattern on the first surface of the piezoelectric substrate.

Regarding Claim(s) 2, Onishi further teaches forming the on-chip pattern two-dimensionally and cutting a joined substrate having the grinded and polished supporting substrate and the piezoelectric substrate into parts each of which parts has a respective one of the on-chip patterns arranged two-dimensionally (see cutting sequence of Figs. 10D to 10E). Note that the claimed "joined substrate" is read as the joining of supporting substrate 102a and piezoelectric substrate 101a (in Fig. 10B) after each has been grinded or thinned, and subsequently, this joined substrate (e.g. 101a, 102a in Fig. 10B) is cut (as shown in Fig. 10E).

Regarding Claim(s) 3, Onishi further teaches housing each of the parts into a respective cavity formed in a first substrate (e.g. 301 and cross-hatched layers not labeled above 301 in Fig. 11), and sealing the respective cavity with a second substrate (e.g. 305).

Regarding Claim(s) 11 and 13, Onishi further suggests that the supporting substrate can be made of silicon such that it is a silicon substrate (col. 4, lines 47-50) and that the piezoelectric substrate contains a major component of lithium niobate (col. 4, lines 33-37).

Onishi teaches substantially all of the limitations of the claimed manufacturing method except that the step of grinding the third surface of the supporting substrate includes polishing of the third surface (as required by Claim 1). Furthermore, Onishi does not mention that electrode pads are formed on the first surface of the piezoelectric substrate (also required by Claim 1).

It is further noted that what Onishi shows in grinding of the third surface of the supporting substrate opposite to another surface of the supporting substrate (in Fig. 10D) is forming grooves, or grooving. Chou teaches that in forming a groove in a silicon substrate, this can also be called polishing (col. 2, lines 15-24). Chou recites that "grinding" is synonymous with "polishing", to perform the same function of forming grooves in a third surface of a supporting substrate.

It would have obvious to one of ordinary skill in the art at the time the invention was made that grinding of the third surface of the supporting substrate of Onishi is a form of both "grinding and polishing" as taught by Chou, since the terms of "grinding" and "polishing" and synonymous with each other and since both Onishi and Chou are performing the very same function of grinding and polishing of the third surface, i.e. forming grooves.

Kawaura teaches that electrode pads (e.g. P_1, P_2, P_3 or P_4) can be formed with comb-shaped electrodes to provide an electrical connection and signal to the on-chip pattern of electrode pads and comb shaped electrodes on the surface acoustic wave device (col. 3, lines 20-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Onishi by adding the electrode pads to the on-chip

pattern, as taught by Kawaura, to positively provide an electrical connection and signal to the surface acoustic wave device and allow the device to operate.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Onishi et al, Chou, and Kawaura et al, as applied to Claims 1 through 3 above, and further in view of EP'756.

Onishi, as modified by Kawaura and Chou, discloses the claimed manufacture method as relied upon above. The modified Onishi method does not teach subjecting one of the joining surfaces of the first and second substrates to a surface activation process that uses plasma and oxygen.

It is noted that sealing of the first and second substrates of Onishi is accomplished by soldering.

EP'756 teaches that substrates, prior to being joined (by soldering), can be cleaned in a preliminary step with a surface activation process of plasma and oxygen (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Onishi by including a surface treatment process of plasma and oxygen on the surface of either the first or second substrate, as taught by EP'756, to provide a clean surface for joining of the first and second substrates (by soldering).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Onishi et al, Chou, and Kawaura et al, as applied to Claim 1 above, and further in view of Romanofsky.

Onishi, as modified by Kawaura and Chou, discloses the claimed manufacture method as relied upon above, further including that the supporting substrate can be made of silicon. The

modified Onishi method does not teach that the resistivity of the supporting substrate with silicon is 100 Ω - m.

Romanofsky teaches that forming a substrate using high resistivity silicon provides the substrate with a resistivity of 1000 Ω - cm (equal to 100 Ω - m) and is advantageous because of the semiconductor properties (col. 8, lines 50+).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the supporting substrate of Onishi by forming the supporting substrate with high resistivity silicon, as taught by Romanofsky, to advantageously provide the supporting substrate with a resistivity of 1000 Ω - cm (equal to 100 Ω - m) and semiconductor properties.

Response to Arguments

7. In light of the embodiment of Figures 10A through 10E of Onishi et al and the newly cited reference to Chou, the applicant(s) arguments filed on March 20, 2007 have been considered to be fully met as explained in the rejections above.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Dexter Tugbang whose telephone number is 571-272-4570. The examiner can normally be reached on Monday - Friday 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Dexter Tugbang/
Primary Examiner
Art Unit 3729

May 24, 2007